OIPE
SEP 14 2005
PATENT & TRADEMARK OFFICE

(1/11)

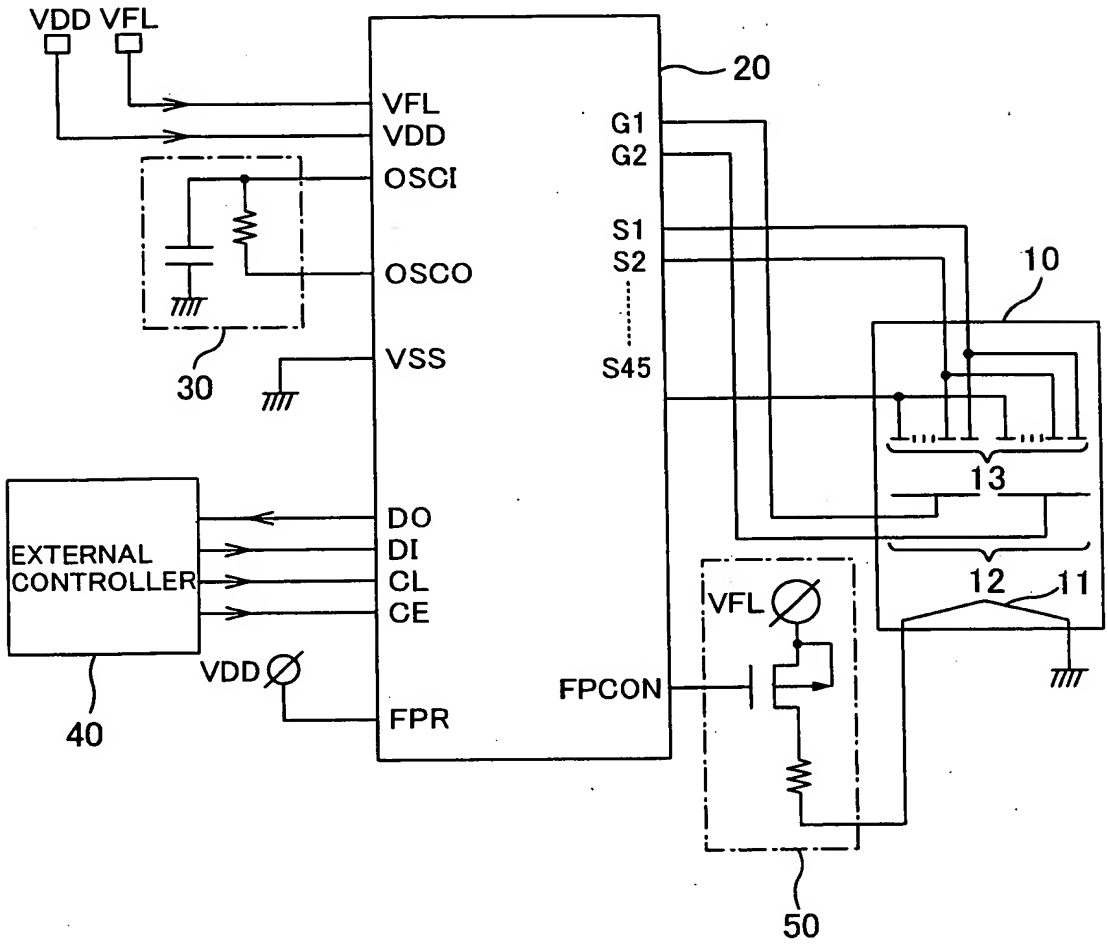

FIG.1

(2/11)

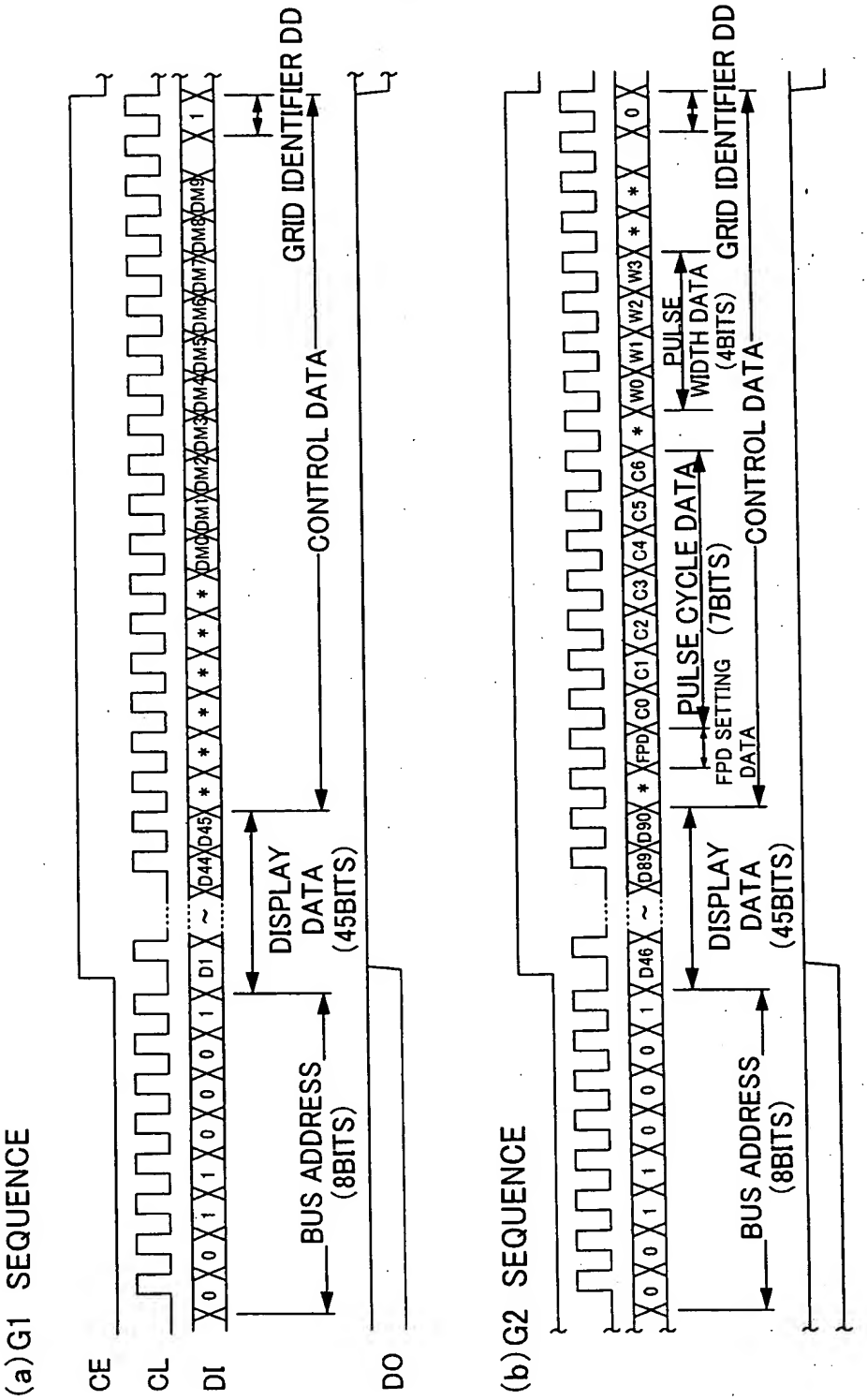
(a) G1 SEQUENCE
CE
CL
DI
DO
BUS ADDRESS (8BITS)
DISPLAY DATA (45BITS)
CONTROL DATA
GRID IDENTIFIER DD
(b) G2 SEQUENCE
BUS ADDRESS (8BITS)
DISPLAY DATA (45BITS)
FPD SETTING DATA
PULSE CYCLE DATA (7BITS)
PULSE WIDTH DATA (4BITS)
CONTROL DATA
GRID IDENTIFIER DD

FIG.2

(3/11)

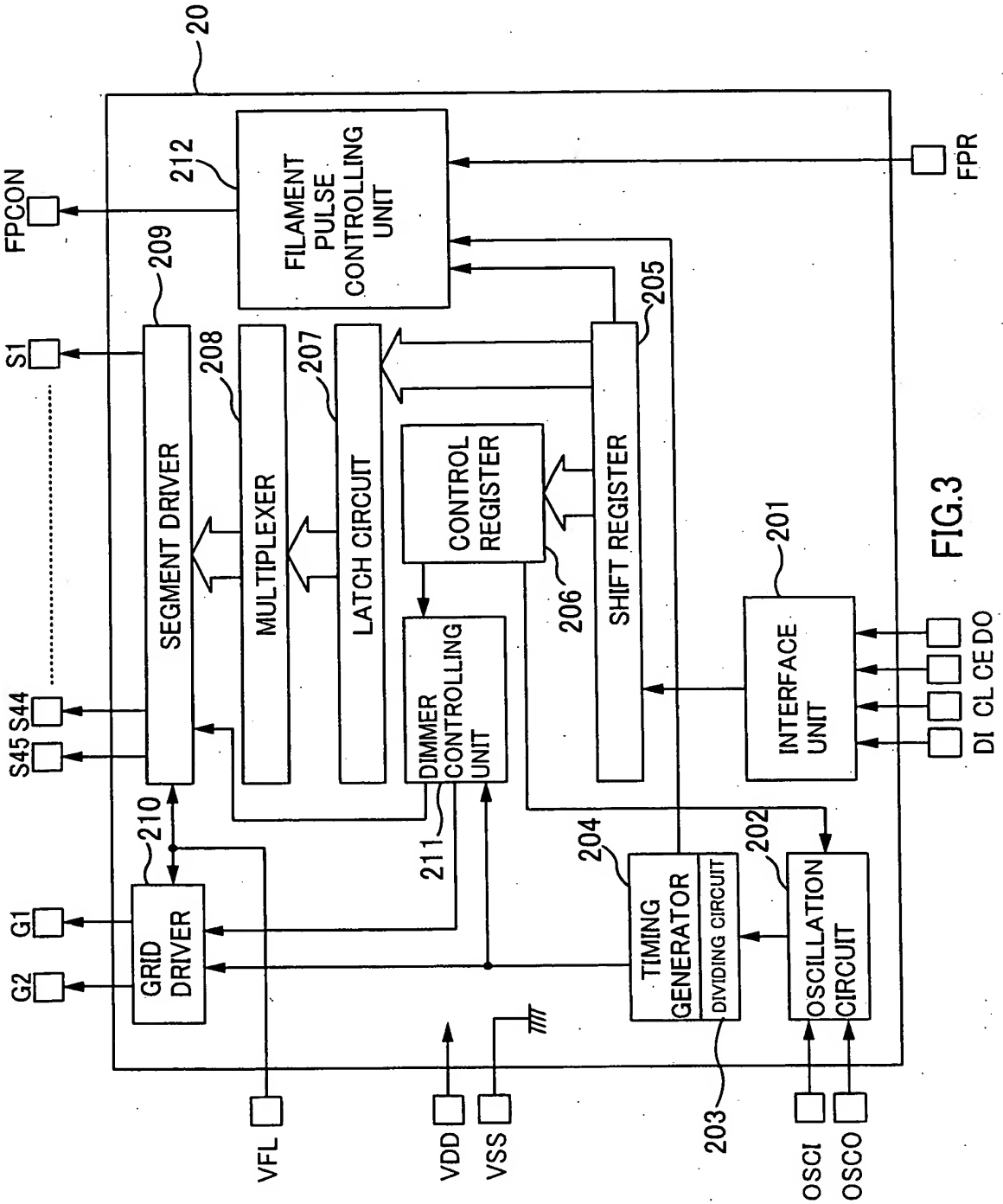
20
FILAMENT PULSE CONTROLLING UNIT
212
FPCON
FPR
209
205
S1
208
207
SEGMENT DRIVER
MULTIPLEXER
LATCH CIRCUIT
CONTROL REGISTER
SHIFT REGISTER
206
201
INTERFACE UNIT
DI CL CE DO
S45 S44
DIMMER CONTROLLING UNIT
210
211
204
202
G1
G2
GRID DRIVER
TIMING GENERATOR
DIVIDING CIRCUIT
OSCILLATION CIRCUIT
VFL
VDD
VSS
203
OSCI
OSCO

FIG.3

(4/11)

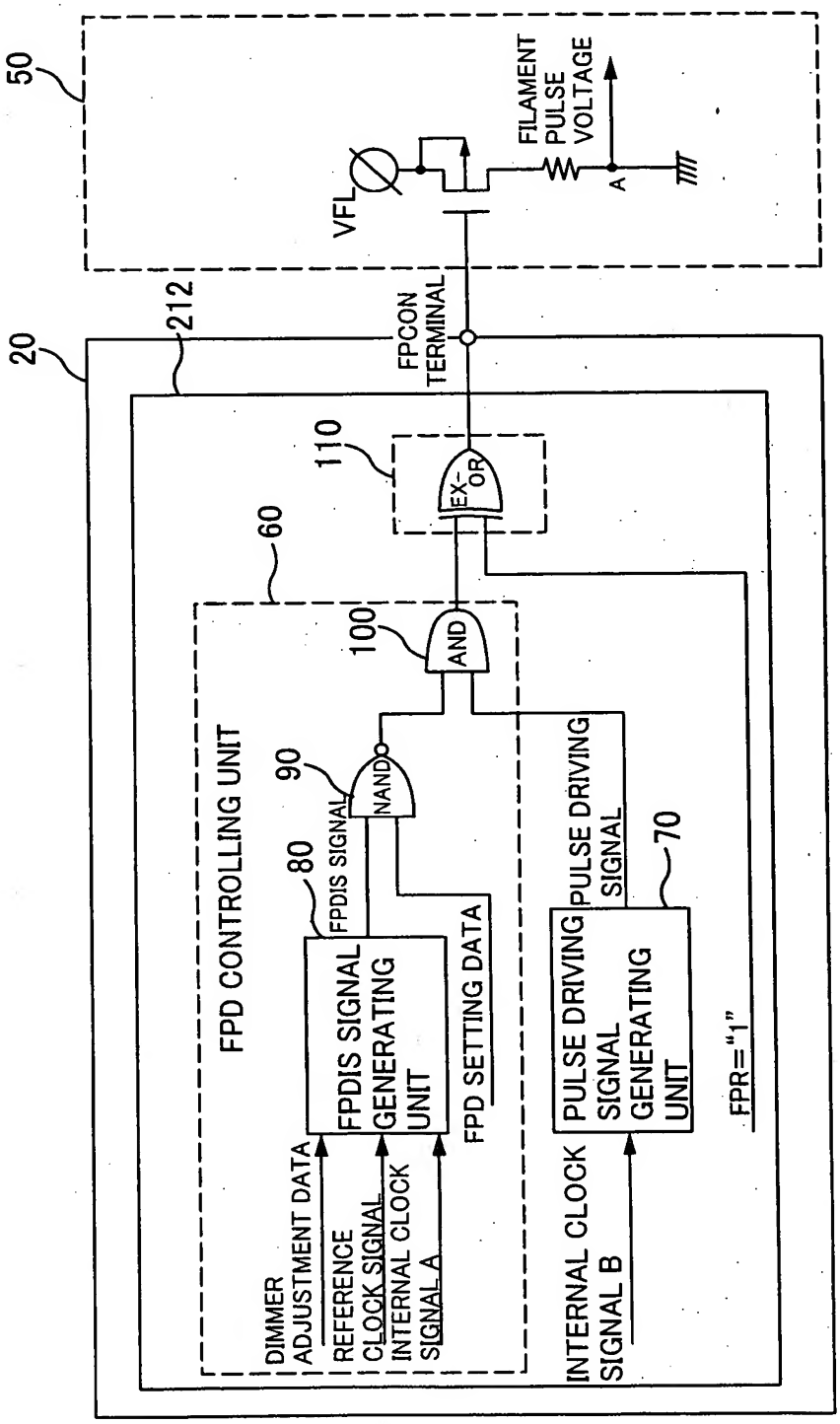
50
FILAMENT PULSE VOLTAGE
VFL
A
20
212
FPCON TERMINAL
110
EX-OR
60
100
AND
90
NAND
FPD CONTROLLING UNIT
80
FPDIS SIGNAL
FPDIS SIGNAL GENERATING UNIT
FPD SETTING DATA
PULSE DRIVING SIGNAL
70
PULSE DRIVING SIGNAL GENERATING UNIT
FPR="1"
DIMMER ADJUSTMENT DATA
REFERENCE CLOCK SIGNAL
INTERNAL CLOCK SIGNAL A
INTERNAL CLOCK SIGNAL B

FIG.4

(5/11)

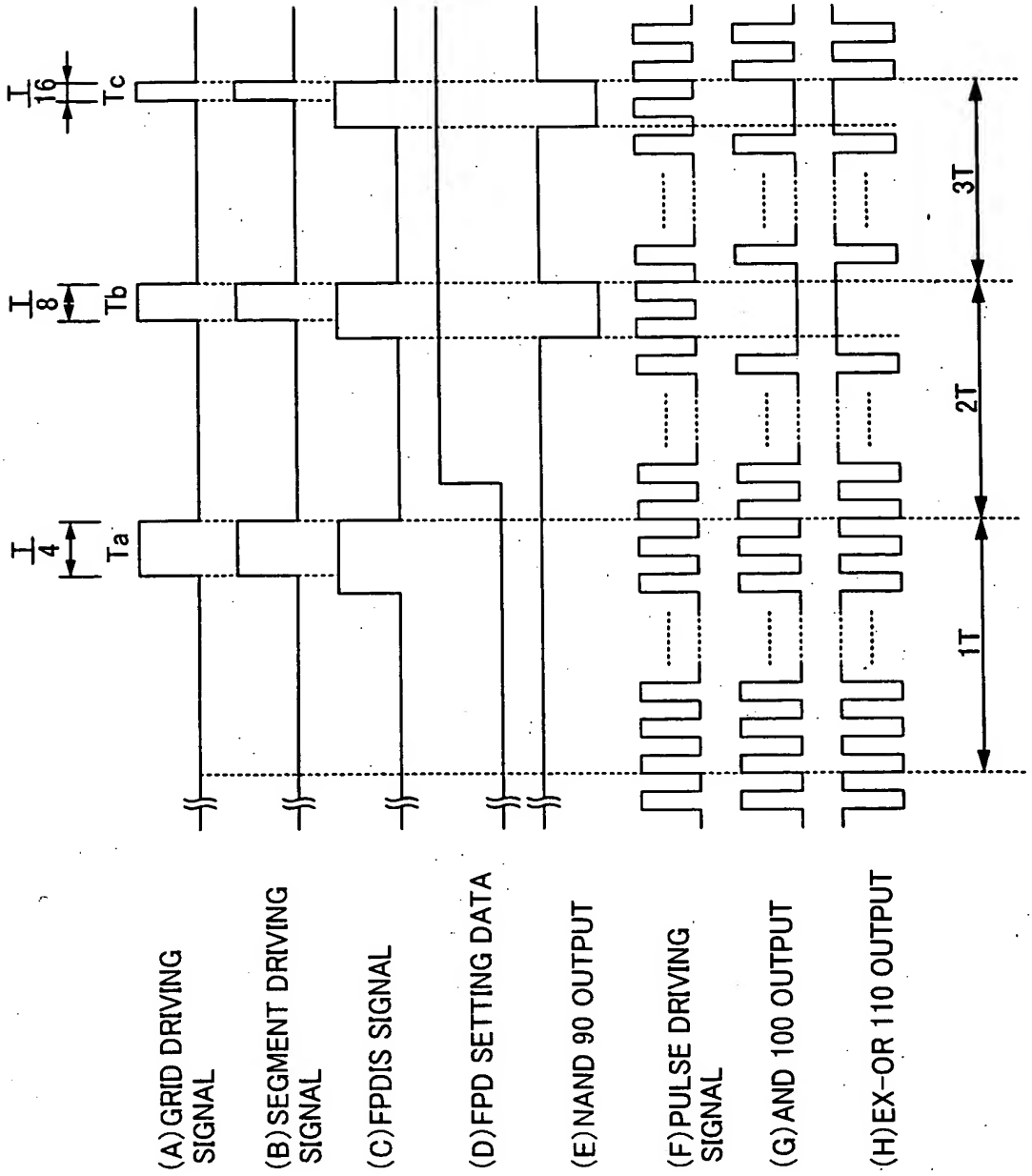
1/16 Tc
1/8 Tb
1/4 Ta
3T
2T
1T
(A) GRID DRIVING SIGNAL
(B) SEGMENT DRIVING SIGNAL
(C) FPDIS SIGNAL
(D) FPD SETTING DATA
(E) NAND 90 OUTPUT
(F) PULSE DRIVING SIGNAL
(G) AND 100 OUTPUT
(H) EX-OR 110 OUTPUT

FIG.5

(6/11)

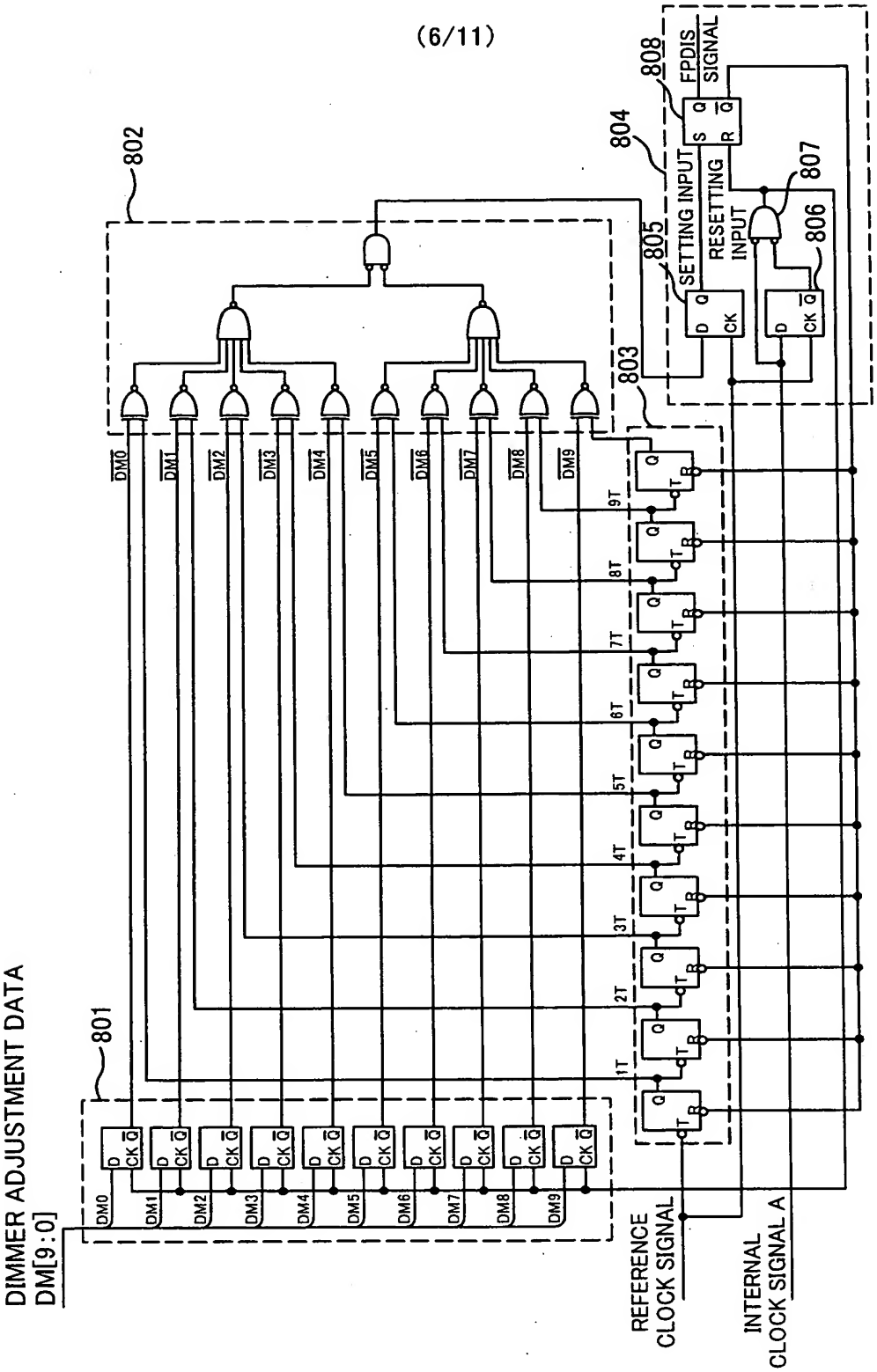
DIMMER ADJUSTMENT DATA
DM[9:0]
801
802
803
804
805
806
807
808
FPDIS SIGNAL
SETTING INPUT
RESETTING INPUT
REFERENCE CLOCK SIGNAL
INTERNAL CLOCK SIGNAL A
DM0
DM1
DM2
DM3
DM4
DM5
DM6
DM7
DM8
DM9
1T
2T
3T
4T
5T
6T
7T
8T
9T

FIG.6

(7/11)

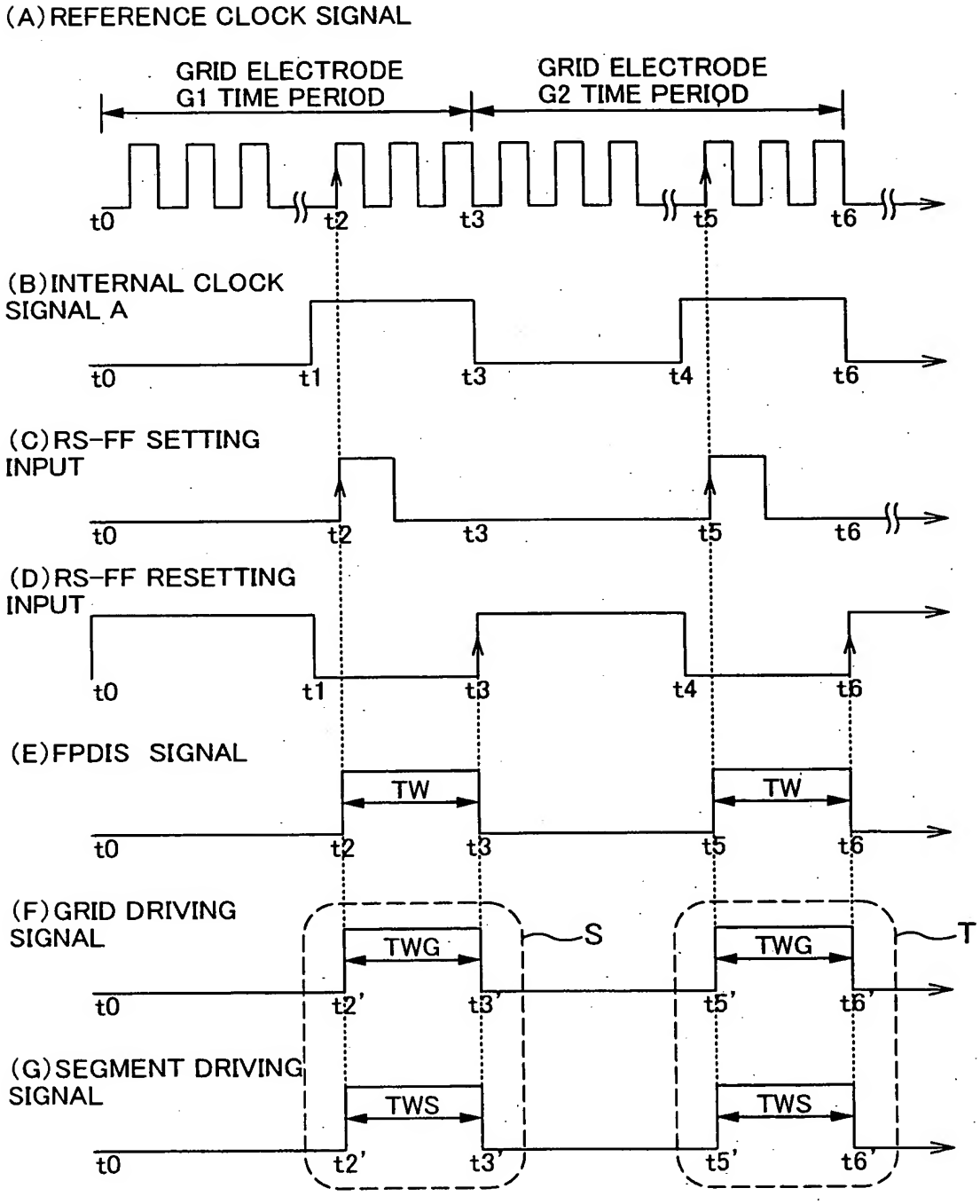
(A) REFERENCE CLOCK SIGNAL
GRID ELECTRODE G1 TIME PERIOD
GRID ELECTRODE G2 TIME PERIOD
t0
t2
t3
t5
t6
(B) INTERNAL CLOCK SIGNAL A
t0
t1
t3
t4
t6
(C) RS-FF SETTING INPUT
t0
t2
t3
t5
t6
(D) RS-FF RESETTING INPUT
t0
t1
t3
t4
t6
(E) FPDIS SIGNAL
TW
TW
t0
t2
t3
t5
t6
(F) GRID DRIVING SIGNAL
TWG
TWG
S
T
t0
t2'
t3'
t5'
t6'
(G) SEGMENT DRIVING SIGNAL
TWS
TWS
t0
t2'
t3'
t5'
t6'

FIG.7

(8/11)

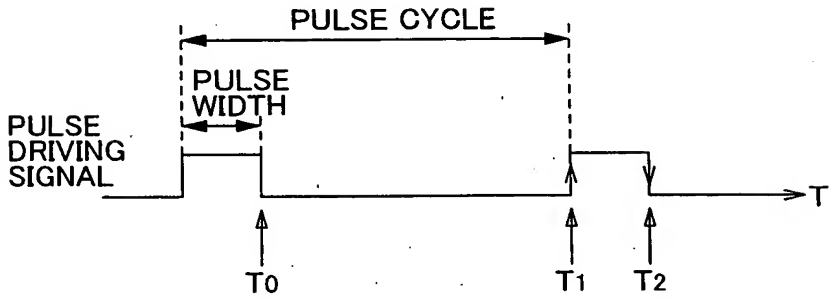

FIG.8

W3	W2	W1	W0	VALUE SET FOR Wn	FPC PULSE WIDTH
0	0	0	0	—	—
0	0	0	1	3	3/fosc
0	0	1	0	4	4/fosc
~					~
0	1	1	0	8	8/fosc
~					~
1	1	1	0	16	16/fosc
1	1	1	1	17	17/fosc

FIG.9

C6	C5	C4	C3	C2	C1	C0	VALUE SET FOR Cn	FPC PULSE CYCLE
0	0	0	0	0	0	0	—	—
0	0	0	0	0	0	1	—	—
0	0	0	0	0	1	0	4	4/fosc
0	0	0	0	0	1	1	5	5/fosc
~								~
1	0	0	0	1	1	0	72	72/fosc
~								~
1	1	1	1	1	1	0	128	128/fosc
1	1	1	1	1	1	1	129	129/fosc

FIG.10

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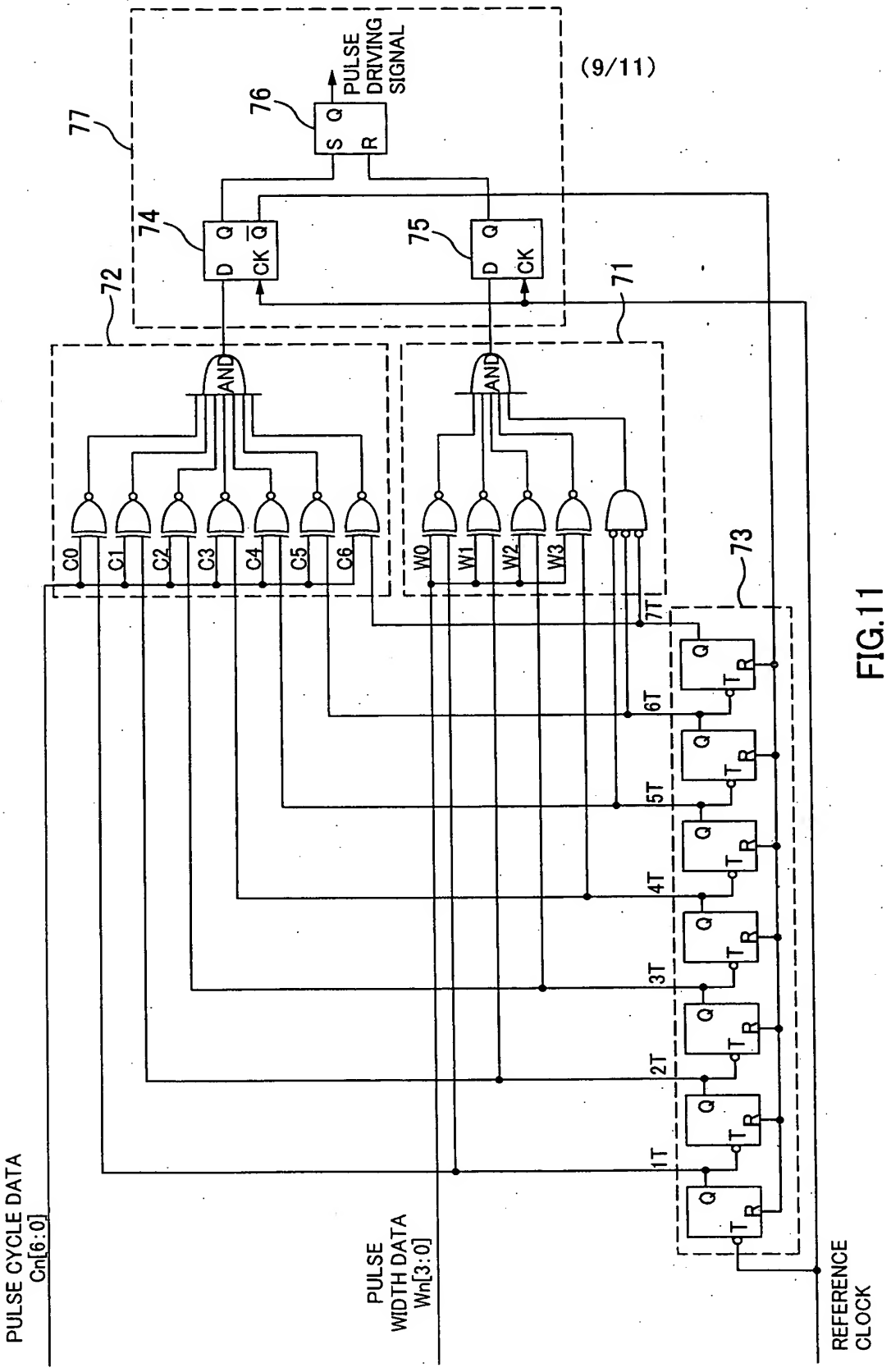

77
76
PULSE DRIVING SIGNAL
S
Q
R
74
75
D
CK
72
71
AND
C0
C1
C2
C3
C4
C5
C6
W0
W1
W2
W3
73
7T
6T
5T
4T
3T
2T
1T
PULSE CYCLE DATA Cn[6:0]
PULSE WIDTH DATA Wn[3:0]
REFERENCE CLOCK

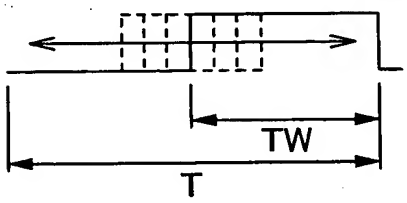
FIG.11

(10/11)

DIMMER ADJUSTMENT DATA

DM9	DM8	DM7	DM6	DM5	DM4	DM3	DM2	DM1	DM0	DIMMER VALUE(TW/T)
0	0	0	0	0	0	0	0	0	0	0/1024
0	0	0	0	0	0	0	0	0	1	1/1024
0	0	0	0	0	0	0	0	1	0	2/1024
					≀					≀
1	1	1	1	1	1	1	1	0	0	1020/1024
1	1	1	1	1	1	1	1	0	1	1021/1024
1	1	1	1	1	1	1	1	1	0	1022/1024
1	1	1	1	1	1	1	1	1	1	IMPOSSIBLE TO SET

(a)



(b)

FIG.12

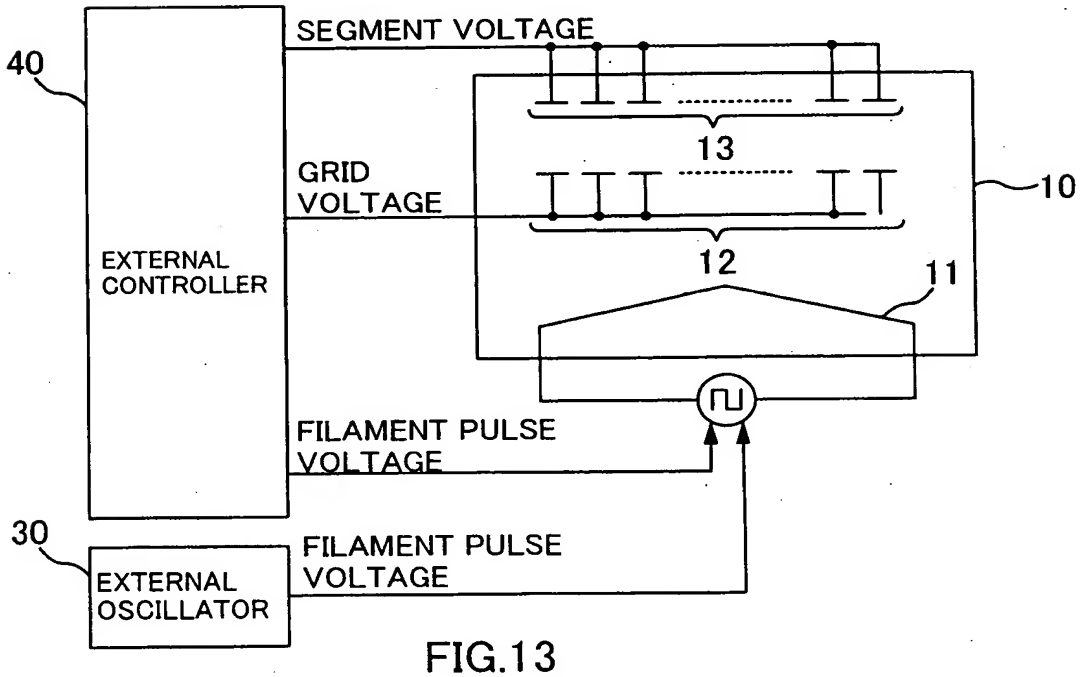


FIG.13

(11/11)

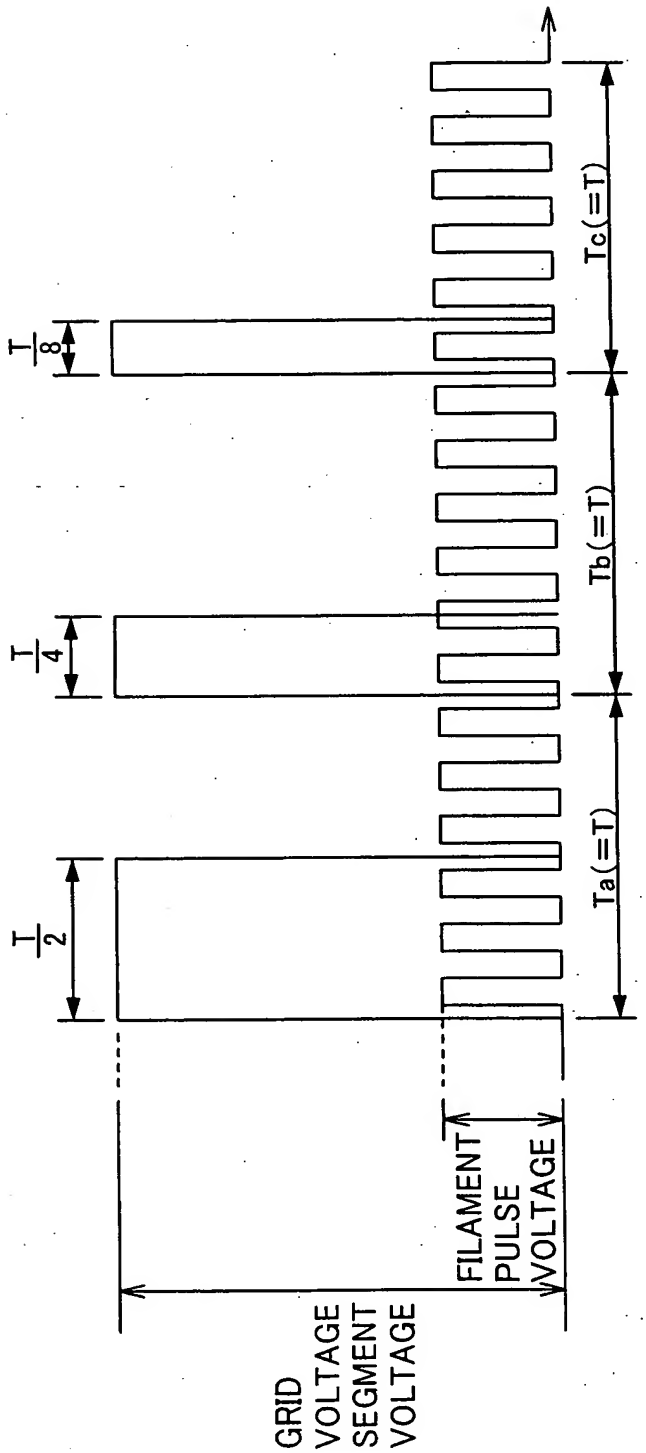

T/8
T/4
T/2
Tc(=T)
Tb(=T)
Ta(=T)
FILAMENT PULSE VOLTAGE
GRID VOLTAGE
SEGMENT VOLTAGE

FIG.14